	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	193	TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating	USPAT; US-PGPUB	2001/10/13 14:00
2	BRS	L2	139	1 and @ad<19980821	USPAT; US-PGPUB	2001/10/13 14:00
3	BRS	L3	136	2 and (phosphorus or P or boron or B)	USPAT; US-PGPUB	2001/10/13 14:02
4	BRS	L4	86	3 and (crystallize or crystallization)	USPAT; US-PGPUB	2001/10/13 14:02
5	BRS	L5	80	4 and (mask or resist or photoresist)	USPAT; US-PGPUB	2001/10/13 14:03
6	BRS	L6	74	5 and channel and source and drain	USPAT; US-PGPUB	2001/10/13 14:03

	Title	Current OR	Current XRef
1	Method of manufacturing a semiconductor device	438/585	134/1.2 ; 438/149 ; 438/151 ; 438/758 ; 438/774 ; 438/974
2	Thin film semiconductor integrated circuit	257/59	257/350 ; 257/72 ; 349/38 ; 349/43
3	Method of promoting crystallization of an amorphous semiconductor film using organic metal CVD	438/486	438/166
4	Method for manufacturing a semiconductor device	438/164	427/561 ; 438/165 ; 438/770 ; 438/771
5	Method for manufacturing semiconductor and method for manufacturing semiconductor device	438/166	438/486
6	Semiconductor device forming method	438/166	438/164 ; 438/486
7	Electro-optical device and thin film transistor and method for forming the same	438/158	438/159 ; 438/160
8	Method for operating an active matrix display device with limited variation in threshold voltages	438/149	117/10 ; 117/44 ; 148/DIG.92 ; 345/205 ; 345/87 ; 345/90 ; 345/92 ; 345/98 ; 438/164 ; 438/166 ; 438/487
9	Method of crystallizing thin films when manufacturing semiconductor devices	438/486	438/149 ; 438/487 ; 438/488
10	Semiconductor device and process for fabricating the same	438/166	117/7 ; 117/8 ; 438/142

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	US 6228751 B1	20010508	22
2	☐	☒	US 6160269 A	20001212	13
3	☐	☒	US 6156627 A	20001205	15
4	☐	☒	US 6150203 A	20001121	17
5	☐	☒	US 6140166 A	20001031	23
6	☐	☒	US 6140165 A	20001031	23
7	☐	☒	US 6124155 A	20000926	19
8	☐	☒	US 6096581 A	20000801	20
9	☐	☒	US 6077758 A	20000620	24
10	☐	☒	US 6071764 A	20000606	23

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Yamazaki, Shunpei , et al.	☒	☐	☐	☐	☐	☐	☐
2		Takemura, Yasuhiko , et al.	☒	☐	☐	☐	☐	☐	☐
3		Zhang, Hongyong , et al.	☒	☐	☐	☐	☐	☐	☐
4		Yamazaki, Shunpei , et al.	☒	☐	☐	☐	☐	☐	☐
5		Ohtani, Hisashi , et al.	☒	☐	☐	☐	☐	☐	☐
6		Zhang, Hongyong , et al.	☒	☐	☐	☐	☐	☐	☐
7		Zhang, Hongyong , et al.	☒	☐	☐	☐	☐	☐	☐
8		Zhang, Hongyong , et al.	☒	☐	☐	☐	☐	☐	☐
9		Zhang, Hongyong , et al.	☒	☐	☐	☐	☐	☐	☐
10		Zhang, Hongyong , et al.	☒	☐	☐	☐	☐	☐	☐

	U	1 [1]	Document ID	Issue Date	Pages
11	☐	☒	US 5994172 A	19991130	32

	Title	Current OR	Current XRef
11	Method for producing semiconductor device	438/151	438/166 ; 438/487

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
11		Ohtani, Hisashi , et al.	☒	☐	☐	☐	☐	☐	☐

DOCUMENT-IDENTIFIER: US 6160269 A
TITLE: Thin film semiconductor integrated circuit

APD:
19971209

ABPL:
A semiconductor device having a pixel provided in an active matrix. Each pixel includes a switching transistor and a pixel capacitor, the switching transistor having a semiconductor region of one conductivity type. An auxiliary capacitor is provided wherein the semiconductor region is one electrode of the auxiliary capacitor. An **insulating** film is provided over the switching transistor and the auxiliary capacitor. Over the auxiliary capacitor is disposed a transparent conductive film which is connected with the semiconductor region through a contact hole provided in the **insulating** film. Additionally, a gate line having a part serving as the other electrode of the auxiliary capacitor is provided.

BSPR:
The present invention relates to a method of manufacturing semiconductor integrated circuits having thin film transistors formed on an **insulating** surface. In the context of the present invention, the term "**insulating** surface" means an **insulating** substrate, an **insulating** film formed thereon, or an **insulating** film formed on a material such as a semiconductor and metal.
More particularly, the present invention relates to semiconductor integrated circuits which employ a metal material mainly composed of aluminum as the material for gate electrodes and gate lines, such as active matrix circuits used for liquid crystal displays.

BSPR:
Thin film transistors (TFTs) have been manufactured using a self-alignment process with the aid of single crystal semiconductor integrated circuit techniques. According to this process, a gate electrode is formed on a semiconductor film through a gate insulation film and impurities are introduced into the semiconductor film using the gate electrode as a **mask**. Impurities can be introduced using methods such as thermal diffusion, ion implantation, plasma doping, and laser doping.

BSPR:
Next, impurities (e.g., phosphorous (**P) or boron (B**)) are implanted on a self-alignment using the gate electrodes/gate lines 406 and 407 as masks according to the ion implantation method, ion doping method, or the like to form impurity regions 408 and 409. In this case, phosphorous is implanted in the impurity region 408 and **boron** is implanted in the impurity region 409. As a result, the former becomes an N-type region and the latter becomes a **P**-type region. (FIG. 4C.)

BSPR:
Specifically, as apparent from the processing steps illustrated, neither introduction of impurities nor laser irradiation takes place once a gate electrode is formed. Therefore, substantially no change occurs in the crystallinity of the region where a **channel** is to be formed.

BSPR:
On the other hand, impurity regions adjacent to a region wherein a **channel** to be formed initially have the same crystallinity as that of the region wherein a **channel** is formed. However, the crystallinity is decreased by the introduction of impurities. Although the impurity regions are repaired by a laser irradiation process performed later, it is difficult to obtain

the initial crystallinity. Especially, the areas of the impurity regions which are adjacent to the active region can not be sufficiently activated because such areas are not likely to be irradiated with laser light. Specifically, since the crystallinity is discontinuous between the impurity regions and the active region, a trap level or the like produces easily. Especially, when impurities are introduced using a method wherein accelerated ions are applied, impurity ions are dispersed into the area under the gate electrode portion and destroy the crystallinity in that area. It has not been possible to activate such an area under a gaze electrode portion using a laser beam or the like because the gate electrode portion blocks the beam.

BSPR:
This equally applies to the gate insulation film. Specifically, while the gate insulation film above the region wherein a **channel** is to be formed remains in the initial state, the gate insulation film above the impurity regions undergoes great changes during steps such as introduction of impurities and laser irradiation. As a result, many traps occur at the boundaries between those regions.

BSPR:
One possible solution to this problem is to perform activation by **irradiating** the substrate on the rear side thereof using a **laser** or the like. According to this method, since the gate lines are not blocked from the light, the boundaries between the active regions and impurity regions are sufficiently activated. In this case, however, the material of the substrate must transmit light. Since most glass substrates can not easily transmit ultraviolet rays having wavelengths of 300 nm or less, for example, a KrF excimer laser (having a wavelength of 248 nm) that excels in mass productivity can not

be used.

BSPR:
Further, during the laser irradiation step as described above, aluminum is heated to a high temperature, although only instantaneously. This has resulted in abnormal growth of aluminum crystals (hillock). Especially, abnormal growth in the vertical direction can cause a short circuit between the aluminum crystals and **wiring** above them.

BSPR:
When ion doping is carried out to dope impurities, another problem arises. Ion doping is a method wherein a gas including impurities for doping (e.g., phosphine (PH.sub.3) if phosphorous is to be doped and diborane (B.sub.2 H.sub.6) if **boron** is to be doped) is subjected to electrical discharge and resulting ions are taken out and emitted using a high voltage.

BSPR:
The present invention solves the above-described problems by activating regions wherein channels are to be formed in addition to impurity regions and gate insulation film using a thermal annealing or an optical annealing process wherein those regions are irradiated by optical energy emitted by an intense light **source** such as a laser or a flash lamp.

BSPR:
The present invention employs a basic configuration as follows. First, a material which serves as a **mask** for the formation of impurity regions is formed on island-like crystalline semiconductor regions and, thereafter, doping impurities are introduced into semiconductor films by means of ion doping or the like using the **mask**. Preferable materials for the **mask** include **insulating** materials such as organic materials, e.g., polyimide and silicon-containing materials, e.g., silicon oxide and silicon nitride and conductive materials

such as metals, e.g., aluminum, tantalum, and titanium and conductive metal nitrides, e.g. tantalum nitride and titanium nitride. If it is desirable to prevent the semiconductor regions from directly contacting the **mask**, a film of silicon oxide or silicon nitride may be formed between them.

BSPR:
Next, the **mask** is removed to form an insulation film which serves as a gate insulation film. Thereafter, a thermal annealing process or an optical annealing process is performed not only to activate the doped impurities but also to improve the characteristics of the interface between the gate insulation film and the regions wherein channels are to be formed and the characteristics of the boundaries between the regions wherein channels are formed and the impurity regions This may be achieved using an optical annealing process or a thermal annealing process alone or using a combination of optical and thermal annealing processes.

BSPR:
A gate electrode may be formed so that it is offset from impurity regions or so that it overlaps with the impurity regions. An offset gate will reduce the leak current of the **TFT**. However, since an offset gate has small amount of current when the **TFT** is turned on, it has the disadvantage of low operating speed. For this reason, offset gates are normally used only in pixel switching TFTs and sampling TFTs of an active matrix circuit, whereas gates which slightly overlap with impurity regions are used for other logic circuits.
Although an overlap gate is not suitable for high speed operations because it has a parasitic capacity, it has no problem in driving an active matrix circuit.

BSPR:
The upper and side surfaces of all or some parts of gate

electrodes and gate
lines thus formed are anodized to form aluminum oxide films having high voltage
withstand characteristics which prevent the gate electrodes and gate lines from
shorting with **wiring** in the layer above them. The formation of such anodic
oxide films is effective for preventing interlayer short circuits especially in
an active matrix circuit wherein may lines intersect with each other. Further,
since aluminum oxide has a high dielectric constant, it can form a capacitor
with a line in the layer above it. Although anodization is normally performed
in an electrolytic solution on an electrochemical basis, it goes without saying
that it may be performed in a low pressure plasma atmosphere as in the
well-known plasma anodization process.

DEPR:
FIGS. 1A to 1D show a first embodiment of the present invention. The present
embodiment represents steps for forming a thin film transistor circuit having
an intersection on an **insulating** substrate. A substrate 101 is a glass
substrate, e.g., a no-alkali borosilicate glass substrate such as the glass of
product No. 7059 available from Corning Corp. A silicon oxide film 102 is
deposited on the substrate as a base oxide film. For example, the silicon
oxide film can be deposited using sputtering or chemical vapor deposition
(CVD). In this case, the film is formed using TEOS (tetraethoxysilane) and
oxygen as material gases according to the plasma CVD method The temperature of
the substrate is 200 to 400.degree. C. The thickness of the base silicon oxide
film is 500 to 2000 .ANG..

DEPR:
Thereafter, a silicon nitride film is formed on the entire surface using a
plasma Cv process to a thickness of 1000 to 6000 .ANG., e.g., 3000 .ANG.. The
thickness is set to a value such that the film can sufficiently

function as a
mask during doping. The silicon nitride film is then etched to form a **mask** 104
for doping. (FIG. 1A.) In this state, **boron** ions are doped using an ion doping
process wherein a gas obtained by diluting diborane (B.sub.2 H.sub.6) with
hydrogen is subjected to electrical discharge and the resulting ions are taken
out using a high voltage to be applied to the substrate. The voltage for
accelerating the ions depends on the thickness of the silicon region. When the
thickness of the silicon region is 1000 .ANG., the adequate voltage is 10 to 30
kV. In this embodiment, the voltage is 20 kV. The dose is 1.times.10.sup.14
to 6.times.10.sup.15 atoms/cm.sup.2, e.g., 5.times.10.sup.14 atoms/cm.sup.2.

DEPR:
Thus, a **P**-type impurity region 105 is formed. The range of the impurity region
illustrated represents only a nominal range, and it goes without saying that
the ions actually wrap around the **mask** due to dispersion of ions and the like.
(FIG. 1B)

DEPR:
Next, the **photoresist mask** 104 is removed, and a silicon oxide film 106 serving
as a gate insulation film is formed to a thickness of 800 to 1500 .ANG., e.g.,
1200 .ANG.. This film is formed using the same method as for the backing
silicon oxide film 102. Then, annealing is performed at 600.degree. C. for 12
to 48 hours, e.g., 24 hours to activate the doped impurities and to improve the
characteristics of the interface between the gate insulation film and the
silicon region. In this step, excessive hydrogen can be removed from the gate
insulation film 106. (FIG. 1C.)

DEPR:
Thereafter, a sputtering process is performed to form an aluminum film
(containing silicon of 1 to 5 percent by weight) having a

thickness of 3000 to
8000 .ANG., e.g., 5000 .ANG.. This film is then etched to form aluminum gate
electrodes/gate lines 107, 108, and 109. The gate electrode 108 is formed to
have an offset configuration with an offset width x of 0.3 to 2 .mu.m. The
gate line 109 is formed above the impurity region. Therefore, the gate
electrode 109 does not function as a gate electrode of a **TFT** but functions as
one of the electrodes of a capacitor. The gate line 107 is electrically
connected to other gate electrodes/gate lines 108 and 109. (FIG. 1D.)

DEPR:
The above-described steps provide a **P-channel** type **TFT** 118 having an offset
structure. Further, a capacity 119 (for which the gate insulation film 106
serves as a dielectric) can be formed adjacent to the **TFT** 118. In the present
embodiment, the **TFT** 118 is a **TFT** used as a pixel switching element or a
sampling **TFT** of an active matrix circuit.

DEPR:
FIGS. 2A to 2F show a second embodiment of the present invention. The present
invention is the same as the first embodiment up to the doping process except
that an element as a catalyst for promoting **crystallization** is added during the
crystallization of amorphous silicon. Therefore, see FIGS. 1A and 1B for the
steps up to the doping step.

DEPR:
Then, after forming a thin nickel acetate film or nickel film, the amorphous
silicon is crystallized by annealing it in a nitrogen or an argon atmosphere at
500 to 580.degree. C. for 2 to 8 hours. In this step, nickel serves as a
catalyst for promoting the **crystallization**. The resulting crystalline silicon
film is etched to form a silicon region in the form of islands.

DEPR:
Thereafter, a plasma CVD process is performed on the entire surface to form a
silicon oxide film having a thickness of 1000 to 6000 .ANG., e.g., 3000 .ANG..
This silicon oxide film is then etched to form a **mask** for doping. Then, a
region where an N-**channel** type **TFT** is to be formed is covered with a
photoresist mask.

DEPR:
With such an arrangement, **boron** ions are doped using an ion doping process.
The doping gas used is diborane diluted with hydrogen (B.sub.2 H.sub.6). The
ions are accelerated by 5 to 30 kv, e.g., 10 kV. The dose is 1.times.10.sup.14
to 6.times.10.sup.15 atoms/cm.sup.2, e.g., 2.times.10.sup.14 atoms/cm.sup.2.
Thus, **P**-type impurity regions 202 and 203 are formed.

DEPR:
When **crystallization** is carried out using a catalyzer element such as nickel as
in the present embodiment, it is observed that some areas remain in an
amorphous silicon state. Such residual amorphous silicon areas can be
completely crystallized by the above-described laser irradiation step.

DEPR:
Thereafter, sputtering is performed to form an aluminum film (containing
scandium of 0.1 to 0.5 percent by weight) having a thickness of 3000 to 8000
.ANG., e.g., 5000 .ANG.. An anodic oxide film having a thickness in the range
from 100 to 300 .ANG. may be formed on the surface of the aluminum in order to
improve the tightness of the contact between the aluminum film and a
photoresist mask during a later step (the step of forming a porous anodic
oxide). This can be achieved by immersing the substrate in an ethyleneglycol
solution containing 1 to 5% citric acid whose pH has been adjusted to about 7

using ammonia and by applying 5 to 20 V to the entire aluminum film.

DEPR:
This film is then etched to form aluminum gate electrodes/gate lines 205, 206, 207, and 208. The gate electrodes/gate lines 205, 206, and 207 overlap impurity regions 201, 202, and 203, respectively, by about 1 .mu.m. The gate line 208 is formed above an impurity region. Therefore, the gate line 208 does not function as a gate electrode of a **TFT** but functions as one of the electrodes of a capacitor. The gate electrodes 205 and 206 are completely electrically insulated from the gate electrodes 207 and 208. The **photoresist** masks 209, 210, 211, and 212 used in the above-described pattern etching step are left as they are. (FIG. 2B.)

DEPR:
Thereafter, the **photoresist** masks 209 through 212 are removed, and another **photoresist** 215 is applied to cover the areas other than the active matrix circuit. Anodization is performed by applying a current to the gate electrodes/gate lines 207 and 208 to obtain fine barrier-type anodic oxide (aluminum oxide) films 216 and 217 having a thickness of 1000 to 2500 .ANG. inside the porous anodic oxides 213 and 214 and on the upper surfaces of the gate electrodes/gate lines 207 and 203. The anodization is carried out by immersing the substrate in an ethyleneglycol solution containing 1 to 5% citric acid whose pH has been adjusted to about 7 using ammonia and by increasing the applied voltage by 1 to 5 V per minute with all the gate lines of the active matrix circuit serving as positive poles. The areas other than the area of the active matrix area are masked by the **photoresist** 215 and are electrically insulated from the active matrix circuit. Therefore, such areas are not anodized. (FIG. 2D.)

DEPR:
The **photoresist** 215 is then removed, and a plasma CVD process is performed
using TEOS as a material gas to form a silicon oxide film 218 as a layer
insulator to a thickness of 2000 to 10000 .ANG., e.g., 5000 .ANG., and a
contact hole is formed in this film. A 5000 .ANG. thick aluminum film is
formed and is etched to form electrodes/lines 219 to 224 on the impurity
regions and gate lines. Although contacts are formed on the gate electrodes
above the silicon regions, in practice, the contacts are formed on the gate
lines in the areas other than the silicon regions.(FIG. 2E.)

DEPR:
The above-described steps provide an N-**channel** type **TFT** 227 and **P-channel** type
TFTs 228 and 229. Further, a capacity 230 (for which the gate insulation film
204 serves as a dielectric) also can be formed adjacent to the **TFT** 229.

DEPR:
In the present embodiment, the **TFT** 229 is a **TFT** used as a pixel switching
element or a sampling **TFT** of an active matrix circuit while the TFTs 227 and
228 are TFTs used in other logic circuits.

DEPR:
FIG. 5 is a block diagram showing an active matrix circuit, a driver circuit
for the same, and other circuits configured using the TFTs described in the
present embodiment formed on a substrate 504. The TFTs 227 and 226 are used in
the logic circuits of X and Y decoder/drivers 515 and 516, a CPU 512, an input
port 510, an X-Y divider 514 and various memories 511 and 513. The **TFT** 229 is
used as pixel switching TFTs 501 of the active matrix circuit 517, sampling **TFT**
of the driver circuits and matrix elements of memories. The capacity 230 is
used as auxiliary capacities 503 of pixel cells 502 of the active

matrix
circuit 517 and as memory elements in memory circuits.

DEPR:
Thereafter, a silicon nitride film 301 having a thickness of 500 .ANG. is deposited on the entire surface using a plasma CVD process. Subsequently, a silicon oxide film having a thickness of 3000 .ANG. is formed on the entire surface again using a plasma CVD process. This silicon oxide film is etched to form masks 302, 303, and 304 for doping. Further, the region where an N-channel type TFT is to be formed is covered with a photoresist mask 305.

DEPR:
With such an arrangement, boron ions are doped using an ion doping. The doping gas is diborane diluted with hydrogen (B.sub.2 H.sub.6). The ions are accelerated by 10 to 50 kV, e.g., 20 kV. The acceleration voltage needs to be increased taking the presence of the silicon nitride film 301 into consideration. The dose is 1.times.10.sup.14 to 6.times.10.sup.15 atoms/cm.sup.2, e.g., 3.times.10.sup.15 atoms/cm.sup.2. Thus, P-type impurity regions 306 and 307 are formed. (FIG. 3A.)

DEPR:
After removing the photoresist mask 305, an ion doping is performed again to dope phosphorous ions. The doping gas is phosphine diluted with hydrogen (PH.sub.3). The ions are accelerated by 10 to 50 kV, e.g., 20 kV. The dose is 1.times.10.sup.14 to 6.times.10.sup.15 atoms/cm.sup.2, e.g., 1.times.10.sup.15 atoms/cm.sup.2. Although the phosphorous is implanted across the entire surface, the P-type impurity regions 306 and 307 remain the conductivity type P because the dose of the phosphorous is smaller than that of the boron which is previously doped. Thus, an N-type impurity region 309 is formed. (FIG. 3B.)

DEPR:
Next, a **photoresist mask** 308, the masks 302 through 304, and the silicon nitride film 301 are removed, and a silicon oxide film 310 which serves as a gate insulation film is formed to a thickness of 800 to 1500 .ANG., e.g., 1200 .ANG.. Then, a beam from a halogen lamp is instantaneously directed to activate the doped impurities and to improve the characteristics of the interface between the gate insulation film and the silicon region.

DEPR:
The intensity of the beam emitted by the lamp is adjusted so that the monitored temperature on the single crystal silicon wafer is 800 to 1300.degree. C. and typically 900 to 1200.degree. C. Specifically, the temperature of a thermocouple embedded in the silicon wafer is monitored and fed back to the infrared light **source**. The temperature is increased at a constant rate of 50 to 200.degree. C./sec. and is decreased on a self-cooling basis to 20 to 100.degree. C.

DEPR:
Intrinsic or substantially intrinsic amorphous silicon well absorbs visible rays, especially, rays of wavelengths shorter than 0.5 .mu.m, and such rays are converted into heat. According to the present invention, rays of wavelengths of 0.5 to 4 .mu.m, are used. Rays having wavelengths in this range can be effectively absorbed by the crystallized intrinsic or substantially intrinsic (the amount of phosphorous or **boron** is 10.sup.17 cm.sup.-3 or less) silicon film and can be converted into heat. Far infrared rays having wavelengths of 10 .mu.m or longer are absorbed by the glass substrate to heat the substrate. However, when most of the rays have wavelengths of 4 .mu.m or shorter, the temperature rise at the glass is very small. That is,

wavelengths of 0.5 to 4
.mu.m are effective for enhancing crystallinity of the silicon film which has
already been crystallized.

DEPR:
As in the second embodiment, areas other than an active matrix circuit are
covered with a **photoresist** 315 and a current is applied to the gate
electrodes/gate lines 313 and 314 to perform an anodization. Thus, an aluminum
oxide film having a thickness of 1000 to 2500 .ANG. is formed, and barrier
type anodic oxide films are formed on the upper and side surfaces of the gate
electrodes/gate lines 313 and 314.

DEPR:
The gate electrodes/gate lines 311 and 312 are formed to overlap the impurity
regions 309 and 306, respectively. On the other hand, the gate electrode/gate
line 303 is formed to have an offset configuration. The present embodiment is
different from the second embodiment in that one side of the impurity region
307 (the side on which a pixel electrode is formed) is in an offset
relationship and the other side is in an overlapping relationship with the
respective gate electrode/gate line. The gate line 314 is formed above an
impurity region. Therefore, the gate line 314 does not function as a gate
electrode of a **TFT** but functions as one of the electrodes of a capacitor.
(FIG. 3D.)

DEPR:
Then, the **photoresist** 315 is removed. A plasma CVD process is performed using
TEOS as a material gas to form a silicon oxide film 316 as a layer insulator to
a thickness of 5000 .ANG., and a contact hole is formed in this film. An
aluminum film having a thickness of 5000 .ANG. is formed and is etched to form
electrodes/lines 317 through 322 on the impurity regions and gate lines. (FIG.

3E.)

DEPR:
The above-described steps provide an N-**channel** type **TFT** 325 and **P-channel** type
TFTs 326 and 327. Further, a capacity 328 (for which the gate insulation film
310 serves as a dielectric) can be formed adjacent to the **TFT** 327. In the
present embodiment, the **TFT** 327 is a **TFT** used as a pixel switching element or a
sampling **TFT** of an active matrix circuit while the TFTs 325 and 326 are TFTs
used in other logic circuits.

DEPR:
The present invention makes it possible to provide a thin film semiconductor
integrated circuit which has less defects and in which gate electrodes and gate
lines are formed of a material mainly composed of aluminum. A **TFT** according to
the present embodiment has high reliability and less deterioration even though
it is manufactured through low temperature processes at 650.degree. C. or
lower. Specifically, there is no significant change in the characteristics of
the transistor after 10 hours or longer in a state wherein the **source** is
grounded and a voltage of +20 V or higher or -20 V or lower is applied to one
or both of the **drain** and the gate. Thus, the present invention is advantageous
from the industrial point of view.

CLPR:
2. The device of claim 1 wherein said **insulating** film comprises silicon
nitride or silicon oxide.

CLPR:
3. The device of claim 1 wherein a dielectric layer of said auxiliary
capacitor comprises the same material as a gate **insulating** film of said
switching transistor.

CLPR:

8. The device of claim 7 wherein said **insulating** film comprises silicon
nitride or silicon oxide.

CLPR:
9. The device of claim 7 wherein a dielectric layer of said auxiliary
capacitor comprises the same material as a gate **insulating** film of said
switching transistor.

CLPV:
an **insulating** film provided over said switching transistor and said auxiliary
capacitor;

CLPV:
a transparent conductive film provided over said auxiliary capacitor and
connected with said semiconductor region through a contact hole provided in
said **insulating** film; and

CLPV:
an **insulating** film provided over said switching transistor and said auxiliary
capacitor;

CLPV:
a transparent conductive film provided over said **insulating** film and connected
with said semiconductor region through a contact hole provided in said
insulating film; and

CLPV:
an **insulating** film provided over said switching transistor and said auxiliary
capacitor;

CLPV:
a transparent conductive film provided over said **insulating** film and connected
with said semiconductor region through a contact hole provided in said
insulating film; and

CLPV:
an **insulating** film provided over said switching transistor and

said auxiliary
capacitor;

CLPV:
a transparent conductive film provided over said **insulating** film and connected
with said semiconductor region through a contact hole provided in said
insulating film;

CLPV:
a **source** region and a **drain** region provided in said transistor provided in said
peripheral circuit;

CLPV:
a **channel** formation region provided between said **source** region and said **drain**
region; and

CLPV:
a gate electrode provided adjacent to said **channel** formation region with a gate
insulating film therebetween,

CLPV:
wherein said gate electrode in said peripheral circuit overlaps with said
source region.

CLPV:
an **insulating** film provided over said switching transistor and said auxiliary
capacitor;

CLPV:
a transparent conductive film provided over said **insulating** film and connected
with said semiconductor region through a contact hole provided in said
insulating film;

CLPV:
a **source** region and a **drain** region provided in said transistor provided in said
peripheral circuit;

CLPV:
a **channel** formation region provided between said **source** region

and said **drain**
region; and

CLPV:
a gate electrode provided adjacent to said **channel** formation region with a gate
insulating film therebetween;

CLPV:
wherein said gate electrode in said peripheral circuit overlaps with said **drain**
region.